Industry's First Open-Source, Current-Based Cell Library Model for Timing, Noise and Power

Accurate cell library models are essential for IC design implementation and sign-off tools. To ensure high accuracy at technology nodes of 90-nm and below, library models must accurately capture the complex transistor behavior of cells. Current-based modeling was introduced and proven in industry in the last few years as an effective way to model nanometer timing effects. However, accurate timing models alone are no longer sufficient because the effects are inter-dependent between timing, noise and power. To comprehensively deal with the inter-dependent timing, noise, and power effects in nanometer ICs, designers need a single current-based library model that enables the concurrent analysis and optimization of issues in all three categories.

The Composite Current Source (CCS) modeling technology is the first in the industry to deliver a complete open-source current based modeling solution for timing, noise and power. Along with the available parsers, characterization/validation tools, and guidelines, this open-source Liberty™ modeling format enables efficient characterization for cell library creators. For IC designers, the CCS modeling technology enables comprehensive nanometer design analysis and optimization for the first time. Designers can reduce design margins and speed design closure by eliminating iterations.

This overview paper describes the nanometer design issues that led to the need for current-based models and shows how CCS models meet the expanding requirements of nanometer designs. An appendix supplies CCS data showing that this modeling technology achieves timing accuracy within 2 percent of SPICE results and noise accuracy within 2 percent of VDD. For detailed information on the CCS modeling technology that goes beyond the scope of this overview paper, please consult the following white papers:

- [Link to the timing white paper](#)
- [Link to the noise white paper](#)
- [Link to the power white paper](#)

Dealing with nanometer issues

The widely available Non-Linear Delay and Power Models (NLDM/NLPM) have served the IC design industry for over 5 years. These models consist of tables capturing a cell’s delay or power for each combination of input slew and output load. At process geometries of 90-nm and below, many new effects can no longer be modeled using this approach. Some of these modeling challenges will be explained in more detail in the next few paragraphs. They include:

- High impedance interconnect
- Miller effect
- Dynamic IR-drop
- Multi-voltage, and Dynamic Voltage and Frequency Scaling (DVFS) design
- Driver weakening
- Temperature inversion
- Increasing variations
To make matters worse, some of these effects are inter-dependent between timing, noise and power. Figure 1 illustrates some of these inter-dependencies. For example, timing and slew rates affect power, which impacts IR-drop, which in turn changes timing. Also, timing impacts signal-integrity, which in turn can because crosstalk induced delay shifts. Another often overlooked fact is that signal integrity can impact power, which in turn impacts IR-drop and timing. Typically designers overlook glitches in a design that do not propagate to a register to cause a functional failure. However, a large number of glitches in a design increase power consumption.

Modeling alternatives
The issues discussed so far, along with many others, prompted the development of the CCS modeling technology. Note that other models have addressed some of these issues using current-based methods, but always relating to timing or noise, or power separately—never all three. These ad-hoc models are typically closed, proprietary and do not provide the comprehensive approach that is vital for improving nanometer design modeling capabilities.

Moreover, some current-based timing models store voltage values for the driver. This provides only limited information about the actual current waveform. In between two (voltage, time) points, only the average current value is known. The true shape of the current waveform cannot be preserved unless a large number of voltage samples are used. Accurate current-based models should rely directly upon current values and include a method for reducing the number of (current, time) points while still retaining accuracy for the every time step in the output pin response.

A unified open, current-based model will foster innovation in the EDA industry to deliver a complete solution that can concurrently analyze and optimize a design for timing, noise and power.

The CCS solution
The CCS modeling technology consists of a single Open-Source Liberty library that covers current-based modeling for timing, noise and power along with all the necessary tools and guidelines for accurate library generation and validation, as shown in figure 2. This complete modeling solution will simplify and accelerate the adoption of this new technology.

CCS models include data specifically targeted at characterizing a cell’s timing, noise, and power behavior. Because CCS is current-based, it enables both temperature and voltage scaling of all cell behavior. This scaling capability can be applied to timing, noise and power and is more sophisticated than conventional interpolation, thus improving accuracy. The ability to scale accurately for voltage and temperature reduces the number of library corners that must be characterized and greatly simplifies low power design (e.g. multi-voltage and DVFS designs) flows in addition to enabling new capabilities such as IR-Drop delay analysis.

CCS timing
Timing modeling with CCS is composed of a driver model and a receiver model, as shown in figure 3. The driver model is a time- and voltage-dependent current source. Because this current source’s drive resistance is essentially infinite, the model provides high accuracy even when the drive resistance is much lower than the interconnect impedance.

The CCS receiver model consists of two capacitances, allowing dynamic adjustment of capacitance during the transition. The capacitance values can also be dependent on input slew, output load and state of the cell.
The cell response (output voltage waveform) for a characterized input slew and output load can be easily determined by integrating the current waveform. When the cell is driving a detailed RC network, data from multiple characterized current waveforms (for different output load values) are used to determine the current dynamically during the transition. Sophisticated scaling of the current waveform enables high accuracy calculation between characterized values of input slew, output load, Vdd and Temperature.

Using these capabilities, CCS timing models achieve accuracy within 2 percent of SPICE. At the same time, the models are simple enough to enable very fast delay calculations for highly complex nanometer designs.

**CCS noise**

CCS noise is a current-based model of cell boundary transistor stages that enables noise analysis with accuracy comparable to SPICE simulation. It provides sufficient information to accurately calculate injected crosstalk noise, propagated noise and the driver weakening. Driver weakening occurs on single stage cells when propagated noise causes the injected noise bumps to increase non-linearly due to the weakening of the driver. The CCS timing receiver model works in conjunction with the CCS noise model to greatly improve noise analysis accuracy by modeling the dependency of receiver capacitance on input transition time and the receiver’s output load capacitance. Noise analysis also benefits from the accurate voltage and temperature scaling mechanism in the CCS technology.

One of the most important benefits of the CCS noise model is the efficient characterization. Unlike NLDM noise models, CCS noise enables signal-integrity analysis tools to calculate noise immunity of the cells on-the-fly. This dynamic computation of noise immunity and noise propagation makes the library characterization runtime 100 times faster than NLDM-Noise without impacting tool runtime. Table 1 shows the library characterization time for a variety of cell libraries on 10 CPUs.

<table>
<thead>
<tr>
<th>Library Technology</th>
<th># of cells</th>
<th>Hrs./corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM 90-nm</td>
<td>595</td>
<td>1.5 hrs</td>
</tr>
<tr>
<td>TSMC 90-nm</td>
<td>747</td>
<td>2 hrs</td>
</tr>
<tr>
<td>IDM#1 90-nm</td>
<td>541</td>
<td>&lt;1 hrs</td>
</tr>
<tr>
<td>IDM#2 90-nm</td>
<td>1304</td>
<td>4 hrs</td>
</tr>
<tr>
<td>IDM#3 65-nm</td>
<td>766</td>
<td>3 hrs</td>
</tr>
</tbody>
</table>

CCS noise deploys the boundary transistor stage modeling technique to achieve high accuracy without having to model every transistor stage in the cell. As shown in figure 4, for single-stage logic (e.g. inverters), the complete stage is described in CCS noise format. In the case of two-stage gates (e.g. AND gates), two connected stages are modeled. For cells with more than two stages, an input stage and an output stage is sufficient to accurately model the behavior of cell for noise analysis since noise does not propagate through such cells.

CCS models provide high accuracy for all crosstalk noise analysis tasks, including noise calculation, noise propagation, and combined noise propagation and noise injection.
**CCS power**

CCS models support the increasing need for power optimization, sign-off power analysis, and power integrity analysis. By capturing current waveforms, CCS-based power analysis has much higher time resolution than analysis with NLPMs. See figure 5. CCS accurately models both static leakage current and dynamic switching current, with full support and straightforward modeling for multi-voltage designs.

Moreover, CCS timing resolution enables accurate analysis of dynamic IR drop—a capability crucial for both power integrity and timing analysis. The model also captures each cell’s equivalent parasitic capacitance and resistance when the cell is not switching, allowing fast calculation of current and power throughout the design, including the IR drop in the power rail network.

CCS provides a comprehensive data format for increasingly sophisticated power optimization and analysis tools, including built-in support for multi-voltage designs in addition to highest accuracy for static and dynamic power.

**CCS model characterization**

Characterizing a cell for CCS models is similar to characterizing NLDMs. The overall characterization process for timing, noise, and power is faster, primarily because CCS enables two orders of magnitude (100X) faster noise characterization runtime than NLDM. Also as mentioned before, the characterization for timing and power can be performed simultaneously.

To speed adoption of CCS Technology, Synopsys provides the following characterization and validation assistance:

- CCS modeling technology white papers
- Open source Liberty format specification
- Characterization guidelines and best-practices documentation
- Push-button library characterization tool (NanoChar) with full CCS support
- Characterization kits that can easily be integrated into existing characterization systems
- Liberty Parser to simplify 3rd party tool support
- Library Compiler that includes CCS syntax checking as well as validation checking
- Library validation guidelines
- SPICE correlation guidelines

**CCS for today’s and tomorrow’s designs**

The CCS modeling technology addresses today’s existing and emerging design requirements—the physical effects of nanometer designs as well as the needs of design strategies such as multiple-voltage domains. In one model, this open-source Liberty format combines the cell data needed to support timing, noise and power analyses that are efficient yet accurate because they begin with current values that are character-
ized for the relevant nanometer dependencies. Because the open CCS format is extensible, these models constitute a foundation that can be enhanced as needed to meet future requirements such as variation-aware or statistical timing analysis.

Appendix

CCS Timing Accuracy Results

CCS timing stage delay and slew results are typically within 2 percent of the golden circuit simulation values. The above figure shows a comparison of CCS timing versus HSPICE for a large number of testcases including highly-resistive nets.

CCS Noise Accuracy Results

Figure showing comparison of CCS Noise analysis results using PTSI versus SPICE.