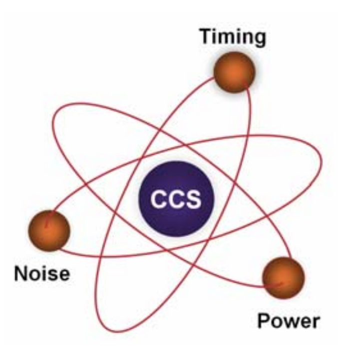
Composite Current Source Model Accuracy Study

CCS timing model accuracy study using PrimeTime and an example design implemented with a 65nm TSMC library



1 Introduction

Accurate delay calculation is critical for timing closure of complex digital designs. At 90nm and below, physical effects present new challenges for delay calculation. Top-level interconnect is becoming more resistive with narrower metal widths, resulting in cases where the interconnect impedance is much greater than the drive resistance of the driving cell. In addition, second order physical effects such as the Miller effect are now becoming first order and must be accounted for in the timing analysis. The concern over power in today's smaller technologies is also presenting new requirements for operation of all or part of the design at lower voltages, increasing the need for analysis over a range of voltages without a unique characterization for each operating point.

A delay model is needed that enables accuracy close to circuit simulation, but with fast calculation to support analysis of the largest designs. The model must support calculation of cell delay, interconnect delay, pin slew (also called "transition time") and input pin capacitance for designs with detailed parasitics. It must also be easily scalable to analyze designs at various operating points with a minimal number of libraries. The Liberty Composite Current Source model for timing (CCS timing) addresses these needs. TSMC has introduced CCS timing libraries to the design community starting at 90-nm for use in today's high performance designs.

This paper discusses an example design implemented using the Synopsys Galaxy platform with TSMC 65-nm CCS timing libraries and presents the accuracy correlation results for unscaled and scaled analysis obtained using PrimeTime and HSPICE.

2 The Ethernet MAC Core

The example design is an open source Ethernet Media Access Control (MAC) core available on www.opencores.org. The MAC is the portion of the ethernet core that handles the CSMA/CD protocol for transmission and reception of frames. The size of the design is approximately 28K gates.

Using the Synopys Galaxy platform, the Ethernet MAC core was implemented with Design Compiler and IC Compiler. The netlist, extracted parasitics, and design constraints were then used as inputs to PrimeTime along with the TSMC 65-nm GPLUS CCS timing libraries to analyze the design. A number of endpoints were chosen at random for accuracy correlation using HSPICE. The method used to validate the library and correlate paths in the design for a 0.90V and 0.80V analysis is discussed in detail in the following sections.

3 CCS timing Characterization

The CCS timing model is an open source model which is part of the Liberty format specification. Characterization guidelines, development tools, and library validation and correlation tools are available to speed the library characterization and qualification process.

To expedite and simplify CCS library qualification, Synopsys provides a new library QA capability part of Library Compiler that can be used to check the completeness and accuracy of all acquired CCS timing models in a library. In addition, Library Compiler can be used in correlation mode to verify the accuracy of the characterization.

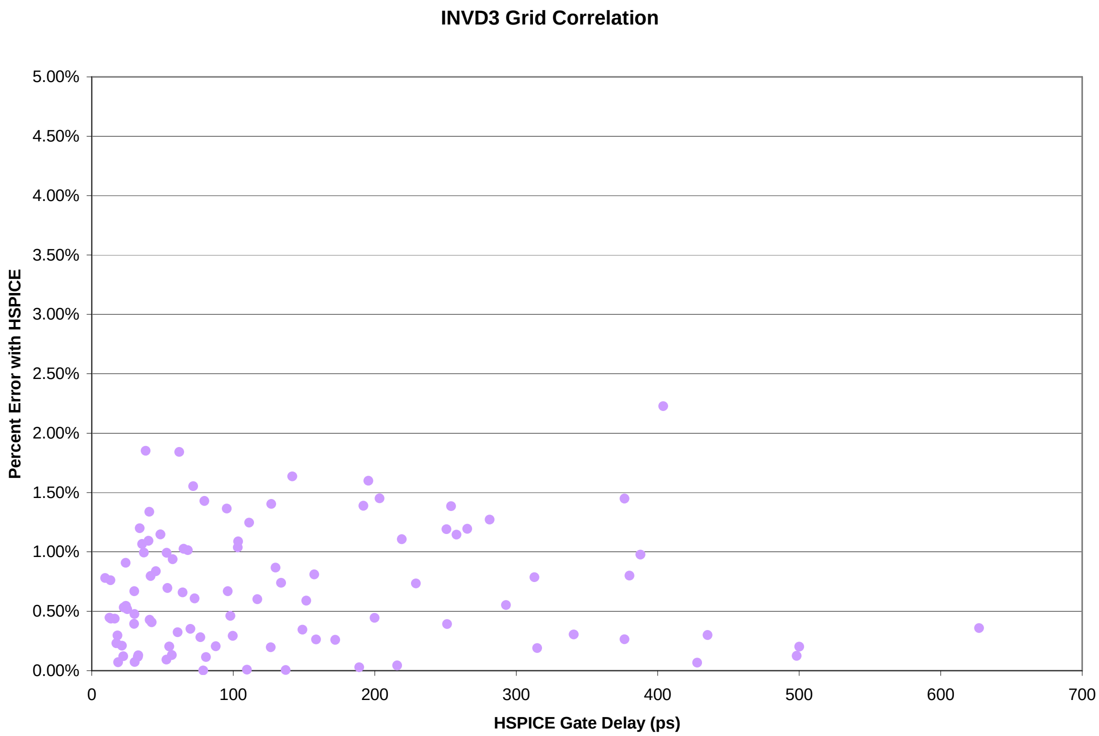
4 CCS timing Library Accuracy

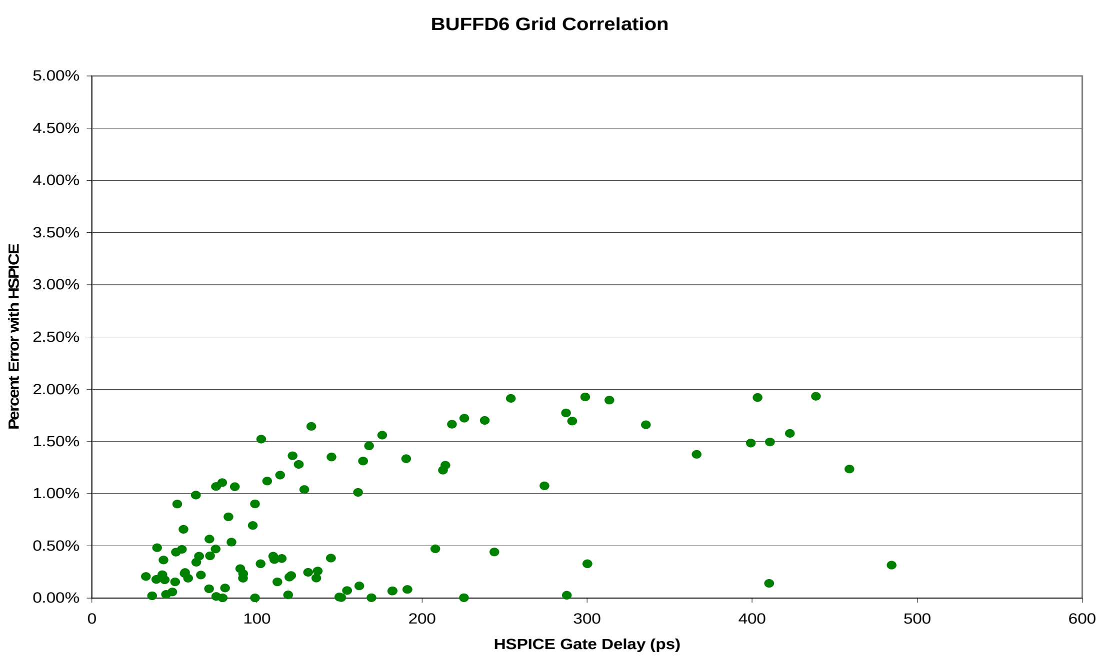
A key component to achieving accurate CCS timing results starts with the library. Several cells from the TSMC library were selected for correlation of the characterization points. In correlation mode, Library Compiler verifies the accuracy of each characterization point of the cell. It sensitizes the cell inputs for each timing arc, creates the parasitic load, and automatically runs the circuit in HSPICE and PrimeTime. Library Compiler sweeps the cell with each characterization input transition and output load and tabulates the results. A simple setup file, the HSPICE subcircuits and models, and the library are all that is needed for LibChecker to automatically generate correlation results.

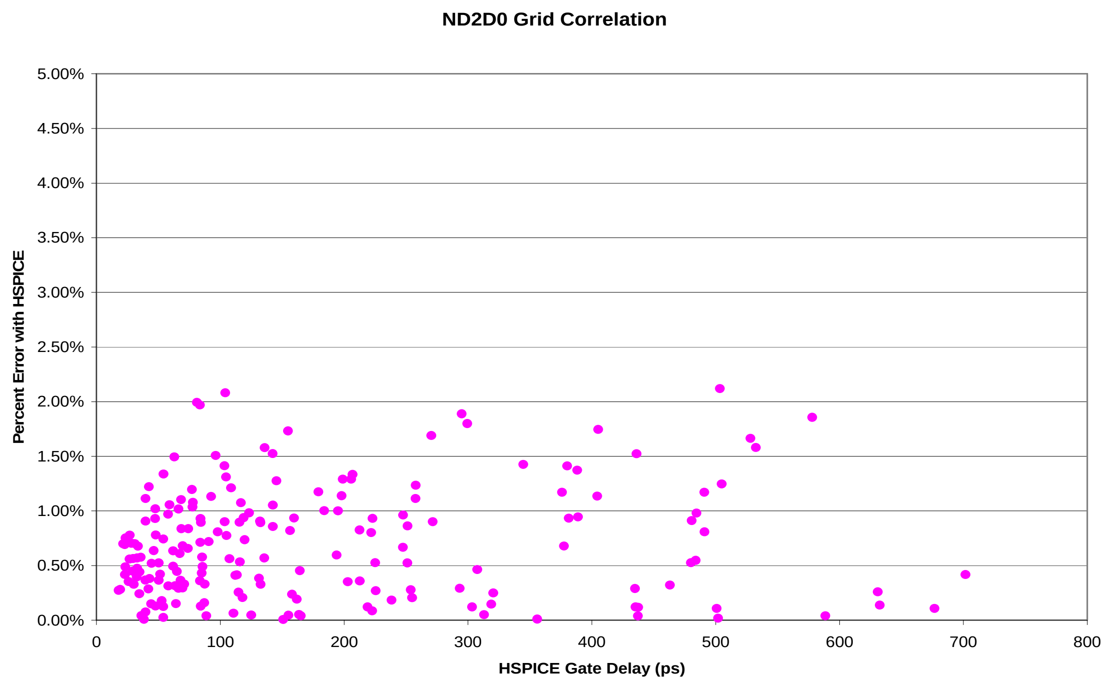
Five cells were chosen for correlation, an inverter, INVD3, a buffer, BUFFD6, a two-input NAND, ND2D0, a three-input NOR, OR3D0, and a clock tree inverter, CKND3. The average error between CCS and HSPICE for all cells is 0.66% with a standard deviation of 0.55%. The average error and standard deviation of each cell is summarized in the table below.

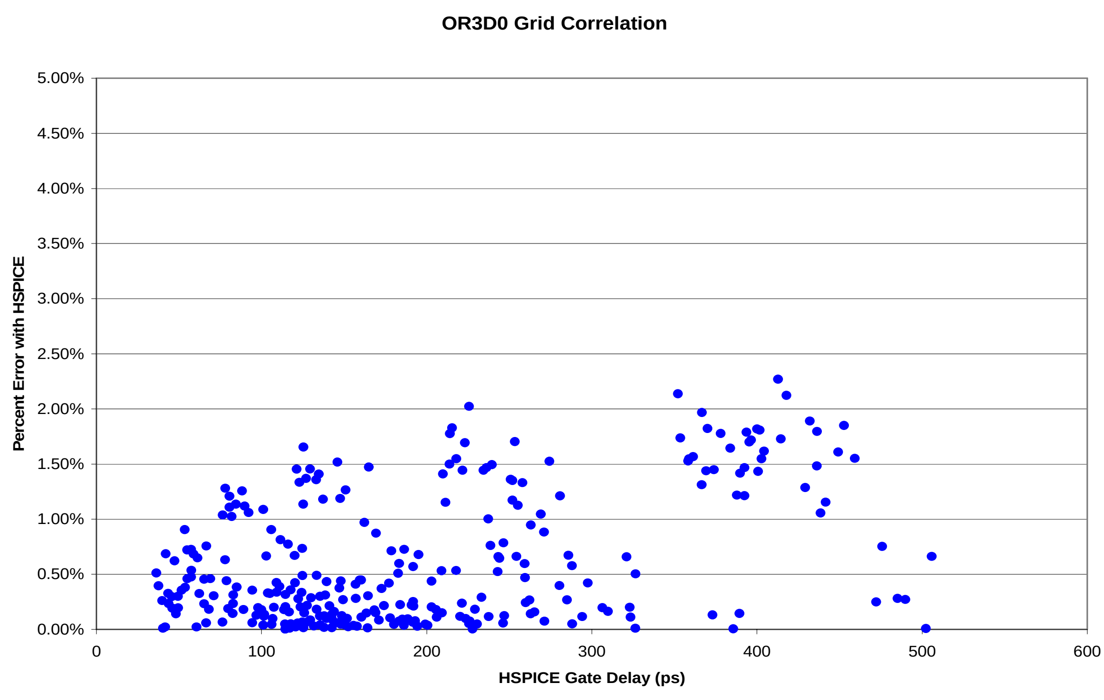
	Average Error	Standard Deviation
INVD3	0.69%	0.51%
BUFFD6	0.70%	0.62%
ND2D0	0.70%	0.50%
OR3D0	0.61%	0.59%
CKND3	0.64%	0.48%

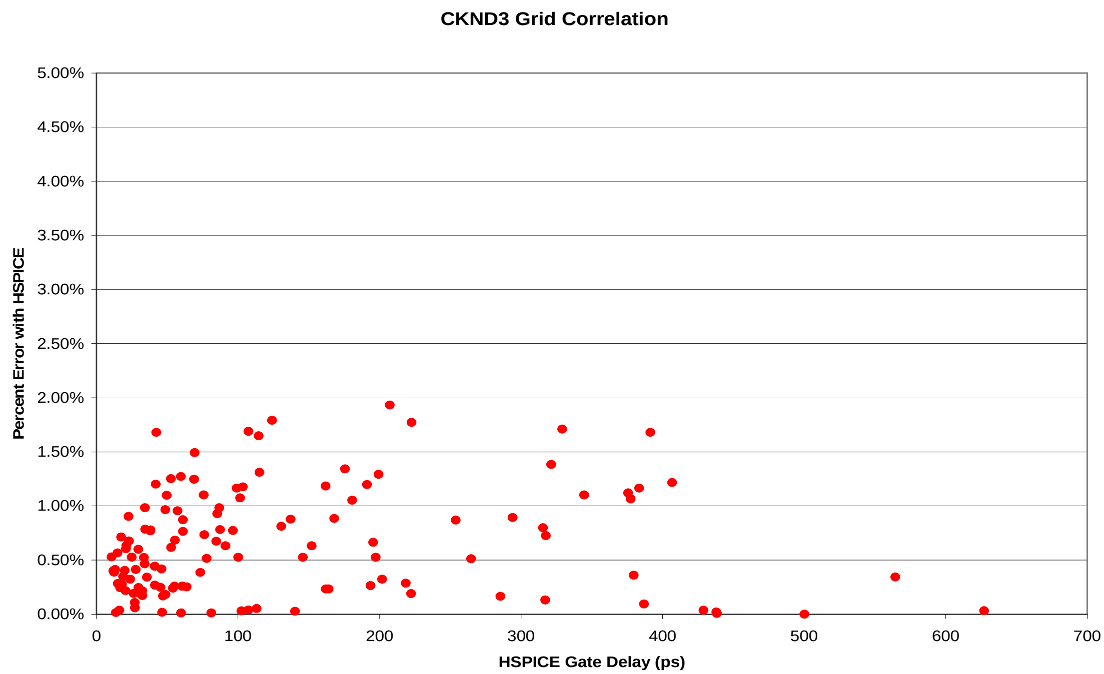
The LibChecker results for the cells are shown in the following figures.


INVD3 Grid Correlation
Percent Error with HSPICE
5.00%
4.50%
4.00%
3.50%
3.00%
2.50%
2.00%
1.50%
1.00%
0.50%
0.00%
0
100
200
300
400
500
600
700
HSPICE Gate Delay (ps)


BUFFD6 Grid Correlation
Percent Error with HSPICE
5.00%
4.50%
4.00%
3.50%
3.00%
2.50%
2.00%
1.50%
1.00%
0.50%
0.00%
0
100
200
300
400
500
600
HSPICE Gate Delay (ps)


ND2D0 Grid Correlation
Percent Error with HSPICE
5.00%
4.50%
4.00%
3.50%
3.00%
2.50%
2.00%
1.50%
1.00%
0.50%
0.00%
0
100
200
300
400
500
600
700
800
HSPICE Gate Delay (ps)

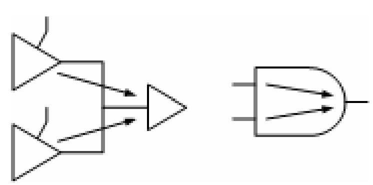

OR3D0 Grid Correlation
Percent Error with HSPICE
5.00%
4.50%
4.00%
3.50%
3.00%
2.50%
2.00%
1.50%
1.00%
0.50%
0.00%
0
100
200
300
400
500
600
HSPICE Gate Delay (ps)



5 PrimeTime Correlation

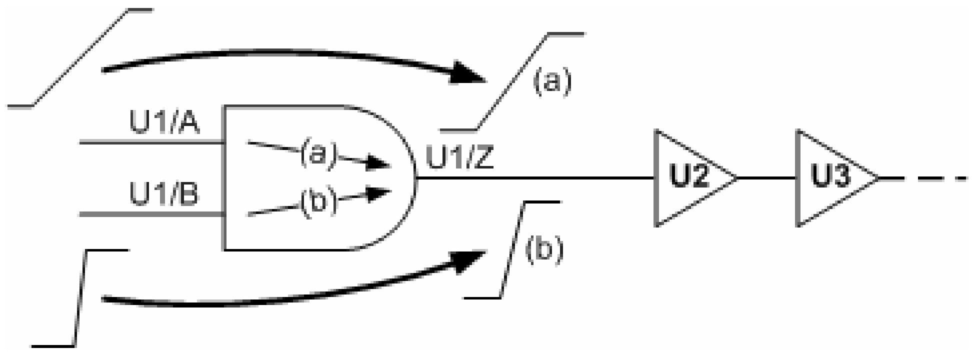
Once confidence in the library model has been established, paths in the design are selected at random for correlation with HSPICE. The correlation procedure is relatively straightforward.

One of the key issues that must be addressed when correlating paths between a static timing analysis tool like PrimeTime and a simulator is worst slew propagation. Whenever two slews arrive at the same point, the static timing tool chooses the worst slew to propagate forward to ensure a conservative analysis. These points are called slew merge points in the design.



Examples of slew merge points

The most common example of a slew merge point is the output of a multi-input combinational gate. In the example below, arcs (a) and (b) of the two-input AND gate each result in a unique slew arriving at the the output pin, U1/Z. To bound the timing analysis, the worst slew is chosen and propagated forward. For max analysis, this is the slowest (numerically largest) slew, and for min analysis, this is the fastest (numerically smallest) slew.



Slew Merge Point Example for Combinational Gate

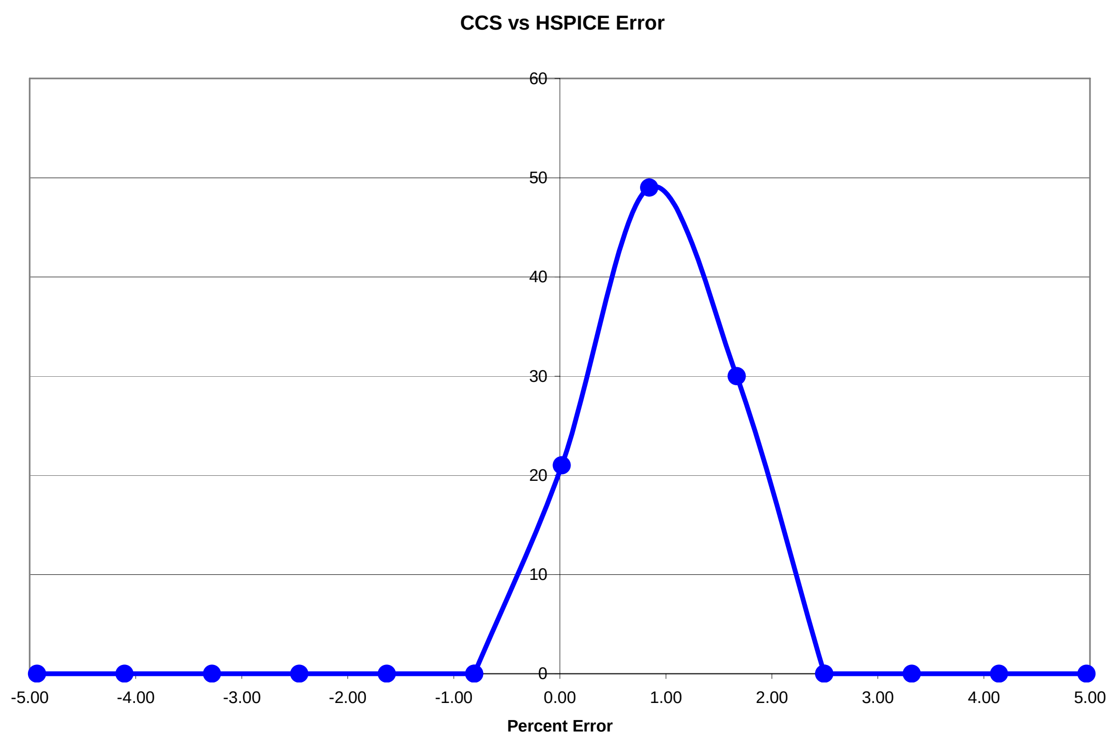
For max analysis, the slew for timing arc (a) is propagated. However, if we are interested in correlating the path for timing arc (b), using the slew from timing arc (a) will introduce inconsistency in the correlation. To remove this effect, PrimeTime provides a path-based analysis function that uses the path-specific slew on the output instead of the worst slew. Path-based analysis should be performed on all paths selected for correlation.

Once the above is done, the path is simulated in HSPICE, and the PrimeTime path-based analysis result is compared to the HSPICE result. As shown in the next sections, the unscaled results at 0.90V and the scaled results at 0.80V using the TSMC 65-nm CCS timing libraries are tightly correlated.

6 Path Correlation Results

A total of 100 data paths were correlated in PrimeTime at 0.90V for the Ethernet MAC Core design using the TSMC 65-nm library. All results were within 2 percent of HSPICE, with a mean error of 0.84% and a standard deviation of 0.82%.

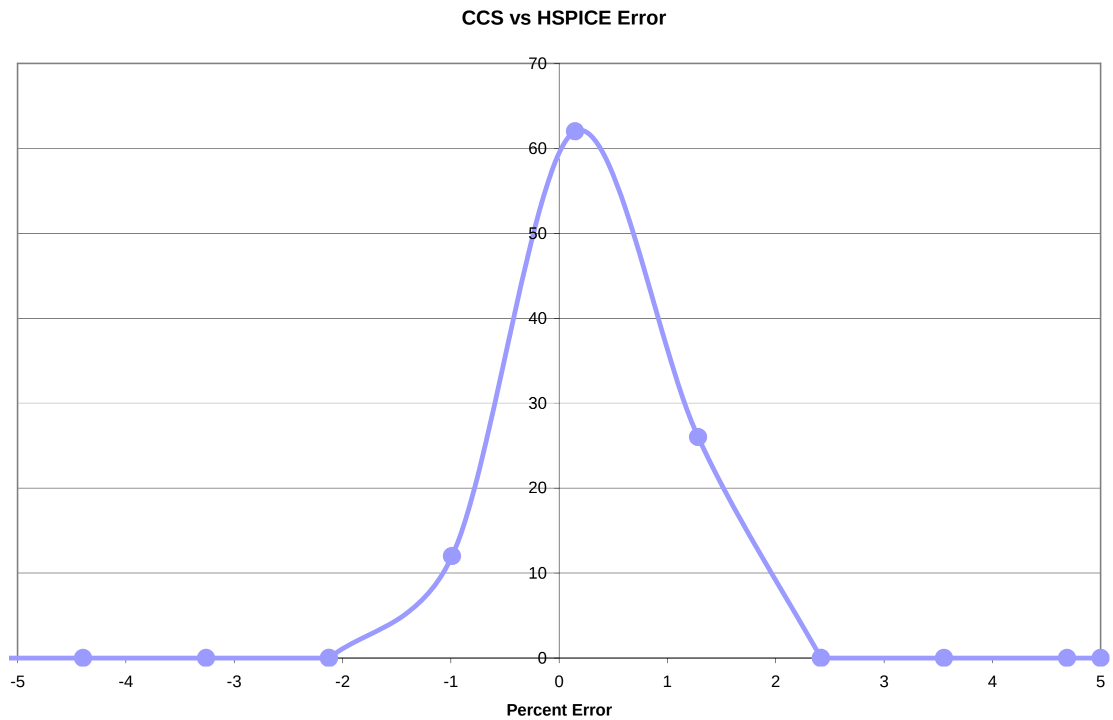
The results are shown in the figure below.



7 PrimeTime Correlation with Voltage Scaling

For a 0.80V analysis, the voltage scaling capability in PrimeTime was utilized with 0.90V and 0.72V TSMC 65-nm GPLUS libraries characterized at the same process corner and temperature. This is easily done by creating a scaling relationship between the libraries in PrimeTime. The scaling relationship allows analysis at any voltage in the 0.72V – 0.90V range.

The same100 data paths were correlated, and the results were within 2.1% percent of HSPICE, with a mean error of 0.15% and a standard deviation of 1.14%. The results are shown in the figure below.



Similarly, voltage and temperature scaling can be performed in PrimeTime with a set of four libraries characterized at two voltages and temperatures with the same process corner.

8 Conclusion

An example design was implemented using TSMC's 65-nm GPLUS libraries. The accuracy of the library was demonstrated showing an average error of 0.66% and standard deviation of 0.55% for several cells. The CCS timing analysis for 100 paths at 0.90V in the Ethernet MAC core design showed an average error of 0.84% and standard deviation of 0.82%. The same 100 paths analyzed at 0.80V using CCS scaling in PrimeTime had an average error of 0.15% with a standard deviation of 1.14%. TSMC CCS timing libraries are ready today to enable designers for high accuracy timing analysis in today's 65-nm designs.