



CCS Power Technical White Paper

Version 3.0

Abstract

This document describes the Synopsys CCS Power model for advanced power and rail analysis and power optimization.

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1 Document History

Revision	Changes
1.0	Initial Version
2.0	Updated minor changes to the document based on review.
3.0	Added gate leakage modeling, asynchronous operation modeling and voltage/temperature scaling support.

2 Introduction

Design closure for today's advanced designs requires delicate balancing between many complex issues. Circuit timing remains critical, but power, test, noise, reliability and manufacturability are also important for design success. Composite Current Source (CCS) modeling extends today's library models to include current waveform data, which allows for more accurate analysis and unification of library data across the toolset.

CCS Power encompasses power and rail analysis and power optimization to provide a complete solution for dynamic and leakage power, dynamic IR drop, and electromigration effects.

This paper describes the fundamental motivation and models incorporated into CCS Power. Additional documents provide details about the library format and the library characterization process.

3 Library-Based Power Analysis

During the operation of a digital circuit, electrical charge is transferred from the power supply pins to the ground pins of cells. The rate at which this charge is transferred corresponds to the power current. Because of the supply voltage difference between the power and ground (PG) pins, the transferred charge exhibits energy dissipation. The rate at which the energy dissipates corresponds to the cell power.

The scope of power analysis is not limited to the calculation of the power dissipation of the design. It covers everything related to calculation of the supply currents, energy and power of all cells in the design. The applications range from average design power calculation to peak supply current calculation for reliability analysis (IR-drop).

3.1 Definitions

A circuit typically dissipates a certain amount of power in the absence of switching activity. The corresponding static power dissipation is referred to as leakage power. When switching activity does occur, the supply current increases. The increase in supply current corresponds to dynamic power dissipation. The total power dissipation is the sum of the static (leakage) and dynamic power contributions.

3.1.1 Leakage Power and Current

The leakage current and leakage power are related:

$$P_{leak} = I_{leak} \cdot V_{supply} \quad (3.1)$$

For multisupply pins consider the general case where there are multiple PG pins. The current of each pin is defined as the current that flows into the cell. For ground pins the current is negative. The total current for all pins must sum up to zero (current conservation). The power of a pin is defined as the product of the pin's current and its voltage relative to the reference node. The total leakage power of the cell is the sum of the leakage power of each pin:

$$P_{leak}(pg - pin) = I_{leak}(pg - pin) \cdot V_{supply}(pg - pin) \quad (3.2)$$

$$P_{leak} = \sum P_{leak}(pg - pin) \quad (3.3)$$

The reference voltage impacts the power of the individual pins, but its value does not matter for the total leakage power because of current conservation. For example, for a single-supply cell (VDD, VSS) it is

$$I_{leak}(VDD) = I_{leak} \quad (3.4)$$

$$I_{leak}(VSS) = -I_{leak} \quad (3.5)$$

$$P_{leak}(VDD) = I_{leak} \cdot V(VDD) \quad (3.6)$$

$$P_{leak}(VSS) = -I_{leak} \cdot V(VSS) \quad (3.7)$$

$$\begin{aligned} P_{leak} &= I_{leak} \cdot [V(VDD) - V(VSS)] \\ &= I_{leak} \cdot V_{supply} \end{aligned} \quad (3.8)$$

3.1.2 Dynamic and Internal Energy

Dynamic energy can be split into two components:

- The switching component associated with charging and discharging the output capacitive load
- The remaining internal component

Internal energy is defined as the dynamic energy minus the switching energy component:

$$E_{\text{int}} = E_{\text{dyn}} - E_{\text{sw}} \quad (3.9)$$

$$E_{\text{sw}} = C_{\text{load}} \cdot V_{\text{supply}}^2 \quad (3.10)$$

Switching energy as previously defined is actually the external switching energy. The actual output capacitance as seen by the driving cell is the sum of the load capacitance and the output pin capacitance.

$$\begin{aligned} E_{\text{sw,tot}} &= (C_{\text{output}} + C_{\text{load}}) \cdot V_{\text{supply}}^2 \\ &= E_{\text{sw,int}} + E_{\text{sw}} \end{aligned} \quad (3.11)$$

For single-stage cells the dynamic energy consists of short-circuit energy and switching energy: in this case the internal energy corresponds to the short-circuit energy and the internal switching energy. For multistage cells, the internal energy also contains short-circuit and total switching energy of the initial stages.

3.2 Dynamic and Internal Current

Dynamic energy that occurs during a transition is derived from the total charge associated with that transition and the voltage over which the charge was transferred:

$$E_{\text{dyn}} = Q_{\text{dyn}} \cdot V_{\text{supply}} \quad (3.12)$$

The charge is the integral of the dynamic current:

$$Q_{\text{dyn}} = \int_0^{+\infty} I_{\text{dyn}}(t) dt \quad (3.13)$$

Similar to internal energy, you can derive the internal current from the dynamic current by subtracting the switching component. The switching current corresponds to the output current that drives the load that is being (dis)charged.

$$I_{\text{int}} = I_{\text{dyn}} - I_{\text{sw}} \quad (3.14)$$

You can easily verify that these equations are consistent with the previous definition of internal energy using

$$\begin{aligned} E_{dyn} &= \int_0^{+\infty} [I_{int}(t) + I_{sw}(t)] dt \cdot V_{supply} \\ &= E_{int} + C_{load} \cdot V_{supply}^2 \\ &= E_{int} + E_{sw} \end{aligned} \tag{3.15}$$

3.3 Types of Analysis

The most accurate way to calculate the cell power in a design is to perform circuit simulation (Spice) and monitor the current waveforms on the PG pins. You can obtain instantaneous power by multiplying by the supply voltage; from which you can easily derive the average and peak power for different parts of the circuit. However, for a digital circuit of reasonable size the simulation time is excessive, so this method becomes unfeasible.

To speed up the analysis you can characterize the power of the individual cells in steady state and in presence of switching events. This characterization is captured in the power library model. A digital simulation of the gate-level netlist yields the various events (switching activity) that occur during the simulation. The power numbers depend highly on the switching activity. You can perform power analysis in two distinct ways:

1. Event-based (dynamic analysis)
2. Average activity-based (static analysis)

Event-based analysis uses a VCD-file or other dynamic switching activity information to identify the events that occurred on the cells in the circuit. For each event, the corresponding energy is obtained from the library data and the power waveform is constructed. For this type of analysis accuracy is the most important criterion.

Average activity-based analysis uses a SAIF-file or other static switching activity information to calculate the average power of events that occurred on the cells in the circuit. For each table in the library every possible event is considered. The likelihood of each event is estimated and the contribution of each event to the average power of the cell is calculated. SAIF-based analysis is used for optimization as well. For this type of analysis performance is a higher priority than accuracy.

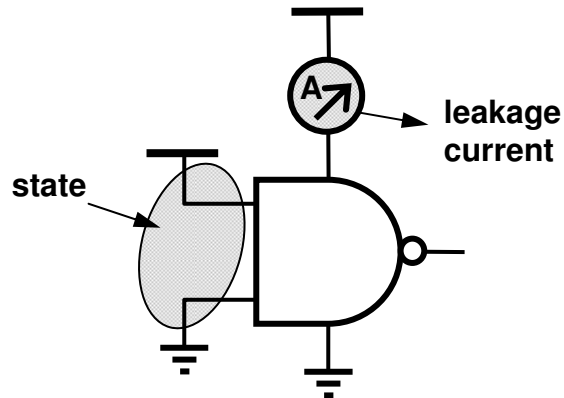
3.4 Table Lookup-Based Models

Modeling leakage power¹ is straightforward because it only depends on the cell state. For combinational cells the state depends solely on the values at the inputs of the cell. For a sequential cell the internal state plays a role too. Typically you can observe the internal state from the outputs of the cell. With the proper initial state a cell can be brought into any state, and a simple DC analysis will yield the leakage current (see figure 3.1). You can derive the leakage power easily by applying equation 3.1. For each possible state (values of inputs and outputs of the cell) the leakage power can be captured in the library model.

The dynamic current waveforms depend on the initial state and the toggling input that causes the event (path dependency). Furthermore, the waveform depends on the transition time of the toggling input and the distributed RC networks of the output loads. When considering the full event from initial (steady) state to the final (steady) state, the energy associated with an event is mainly determined by the capacitive component of the RC load. That is, if you replace the distributed-RC load with a linear capacitance that corresponds to the total capacitance of the RC load, the dynamic energy of the corresponding event is very close to that of the original circuit.

¹ The leakage current and leakage power in this paper, if not specifically distinguished, refer to the intrinsic P-G channel leakage current/power not the combination of channel leakage and gate leakage current/power. Because of this, not all the libraries need to measure gate leakage current. Refer to Chapter 6 for details about leakage current/power.

Figure 3.1: Leakage Current Measurement

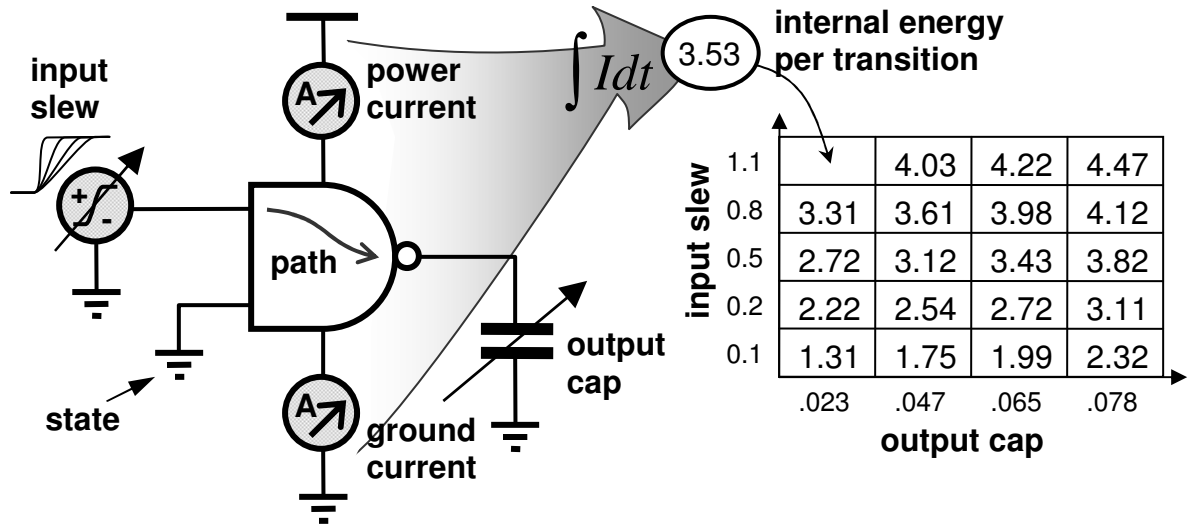


For any given circuit you can obtain the input transition times from (static) timing analysis and you can back-annotate or estimate the output loads with wireload models and input capacitance data that is also available in the library model. You can calculate the switching energy from the output capacitance with equation 3.10. Hence, it makes sense to capture the internal energy as function of the input transition time and the output load. This is the table lookup modeling approach as shown in figure 3.2.

For every state and input pin, simulate the single input event for a number of input transition times and output capacitance combinations. The dynamic energy is obtained by integrating the current and multiplying by the supply voltage (equations 3.12 and 3.13). Finally, you can obtain the internal energy by subtracting the switching component as shown in equation 3.9. The resulting internal energy numbers are stored in a table indexed by the input transition time and the total output load capacitance.

The state dependent (SD) leakage power numbers and the state and path dependent (SDPD) internal energy tables are captured in the NLPM (Non-Linear Power Model) library format. The purpose of this model is to perform post-processing during the modeling phase of characterization to represent the power data in a very compact form that is suitable for consumption by dedicated applications.

Figure 3.2: Dynamic Energy Measurement



The advantages of this approach are

- Compactness of the library
- Speed of leakage and dynamic power analysis

The main disadvantages are

- Limited to dedicated application
- Limited accuracy

An example of the limitations due to storing derived data is the calculation of PG pin specific leakage current. Because leakage current and power are related by the use of equation 3.2, the leakage current can be derived from the leakage power:

$$I_{leak}(pg - pin) = \frac{P_{leak}(pg - pin)}{V_{supply}(pg - pin)} \quad (3.16)$$

For cells with a single ground pin this pin is usually also chosen as the reference pin. As a result, both the supply voltage and the resulting leakage power is zero. In this case you cannot derive the leakage current from equation 3.16. Instead, apply current conservation to calculate the leakage current:

$$\sum_{pg_pin} I_{leak}(pg_pin) = 0 \quad (3.17)$$

Together with equation 3.16 you can find the ground leakage current:

$$\begin{aligned} I_{leak}(ground_pin) &= - \sum_{pg_pin \neq ground_pin} I_{leak}(pg_pin) \\ &= - \sum_{pg_pin \neq ground_pin} \frac{P_{leak}(pg_pin)}{V_{supply}(pg_pin)} \end{aligned} \quad (3.18)$$

Use only current conservation to derive one leakage current at the reference voltage. If the cell has multiple ground pins (such as a state-retention power gating (SRPG) cell with a primary and a backup supply), the leakage current for the individual pins cannot be derived from the leakage power of the cell's supply pins.

Another shortcoming of the NLPM model becomes apparent when considering the application of IR-drop analysis. This requires an exact calculation of the current waveforms as seen on the supply pins. These current waveforms are available during characterization, but only a derived value based on the integrated current is stored in the table. From this table it is impossible to reconstruct the waveform with sufficient accuracy to perform rail analysis. Another important piece of information that is not present in the NLPM model is the equivalent parasitic for non-switching cells. Traditionally, these cells are either totally ignored or represented by their loading capacitance during rail analysis. Either approach results in inaccurate dynamic rail analysis.

4 CCS Power Library Model

The NLPM library model has served its purpose well, but it is clear that the simple table lookup-based model suffers from significant shortcomings that prevent it from being used successfully for a wide range of applications and with advanced design techniques. For this reason, the CCS Power library model was introduced. This model represents the physical circuit properties more closely to the simulated data obtained during characterization with Spice. It is a current-based power model that contains the following features:

- One library format suitable for a wide range of applications (power analysis and optimization; reliability analysis)
- Allows power analysis with much higher time resolution compared to NLPM

- Equivalent parasitics necessary to perform IR-drop analysis
- Standard-cell and macro-cell modeling

4.1 Leakage Power Modeling

Leakage power is modeled as leakage current in the library such that detailed current analysis for multisupply cells with multiple ground pins can be performed. Furthermore, the leakage current does not artificially depend on the reference voltage, as is the case with leakage power. This facilitates voltage scaling by interpolation between libraries.

4.2 Dynamic Power Modeling

Dynamic power modeling with CCS Power is characterized by:

- Current waveforms stored in the library
- Charge can be derived from the current waveform

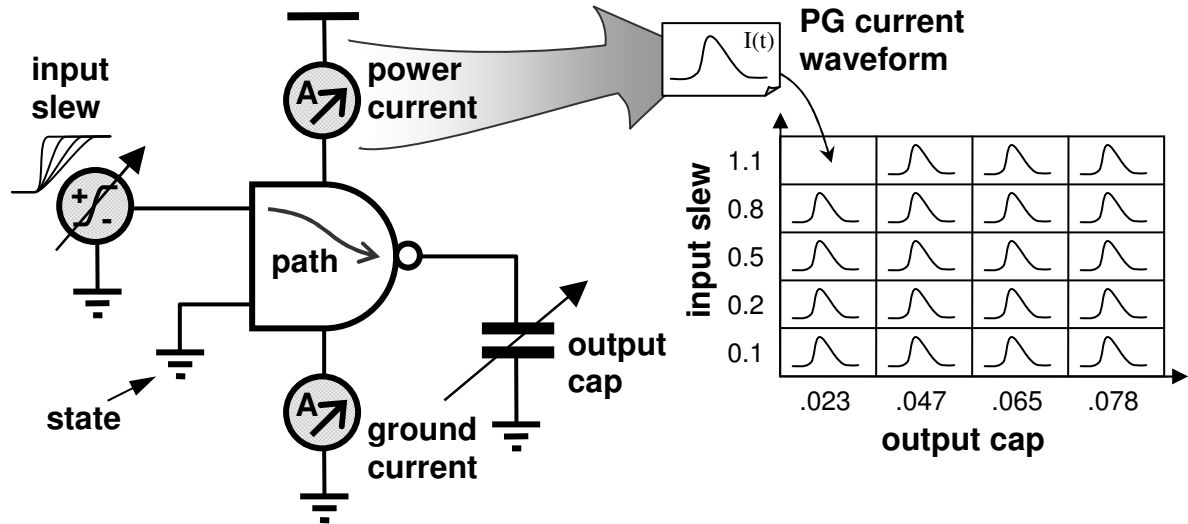
4.2.1 Dynamic Current and Charge

Similar to leakage power data, it is necessary to store dynamic power data in a fashion that is independent of the reference voltage. The equivalent property for energy is the charge, which is the integral of the current waveform. You can derive dynamic energy easily by adding the switching energy. Calculate this component without additional library data with equation 3.10. However, this is no longer the case for the dynamic current waveform: you cannot derive the switching current waveform easily. Therefore, in CCS Power the dynamic current waveform are stored directly, without subtracting the switching component.

4.2.2 Current Waveform

During characterization a current waveform is captured for each combination of input transition time and output loads. The result is stored as a 3D table of current values as a function of input transition time, output capacitance, and time. This is shown in figure 4.1.

Figure 4.1: Dynamic Current Waveform Measurement

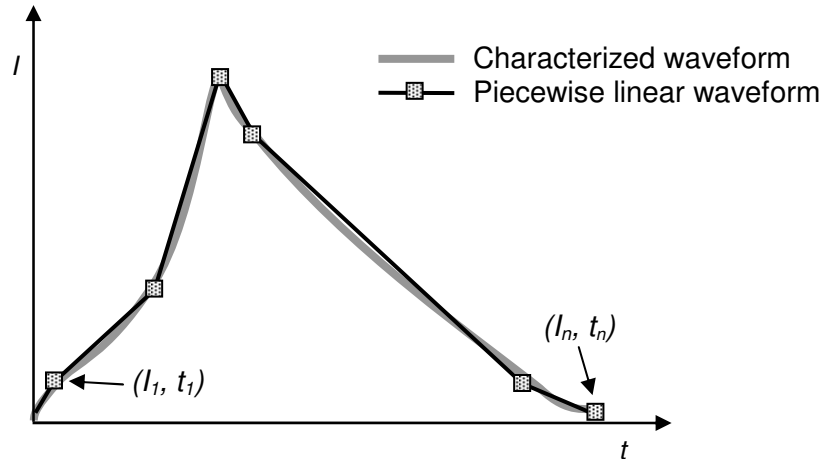


The outcome of the characterization process is a current waveform that is represented as a sequence of (I, t) pairs. Not all points need to be recorded in the library model; missing points can be reconstructed by linear interpolation. The end result is a piecewise linear model as shown in figure 4.2. The highlighted boxes are the actual (I, t) points recorded in CCS Power.

Derive the charge of the dynamic current waveform by numeric integration using the following expression (with $t_0 = 0$ and $I_0 = 0$):

$$Q_{dyn} = \sum_{i=1}^n \frac{1}{2} (I_i + I_{i-1}) (t_i - t_{i-1}) \quad (4.1)$$

Figure 4.2: Piecewise Linear Current Waveform



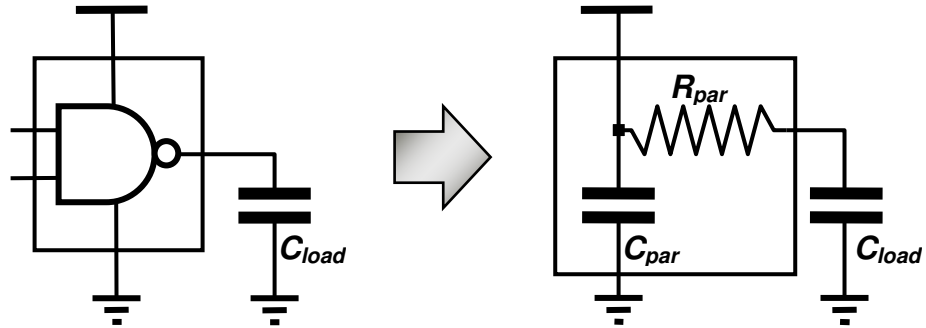
4.3 Equivalent Parasitics

Rail analysis determines the potential IR-drop on power supply pins for non-switching cells in the presence of switching activity in the network. A good approximation is to model the non-switching cells as equivalent small signal networks. The circuits as seen from the power network appear sufficiently linear for a wide frequency range for this first order approximation to be accurate. The simplest model that provides decent accuracy is the PI-model, as shown in figure 4.3.

C_{par} is the PG pin capacitance, which might include well capacitance and channel capacitance. R_{par} is the channel resistance and C_{load} is the loading capacitance of the signal net. The parameters C_{par} and R_{par} are captured in the library model, and C_{load} is stitched during runtime rail analysis.

Equivalent parasitics are state dependent. For each input state an equivalent capacitance, C_{par} is modeled for each PG pin, and an equivalent resistance, R_{par} is captured from each PG pin to each output pin. If one of the channels from the PG pin to the output pin is off, the channel resistance will be very big and you can omit the equivalent resistance because it is assumed to be infinite.

Figure 4.3: Equivalent Parasitics



5 CCS Power Characterization

The CCS Power characterization process is very similar to NLPM characterization:

1. First, the leakage currents are measured with simple DC analysis
2. Next, the dynamic current waveforms are acquired with a transient analysis
3. Finally, the equivalent parasitics is measured with fast AC and DC analysis runs

You can perform most of the characterization for timing and power simultaneously to reduce the characterization runtime.

5.1 Leakage Current

The typical simulation setup for leakage characterization is shown in figure 3.1. This measurement is usually performed as part of the simulation setup for timing analysis.

5.2 Dynamic Current

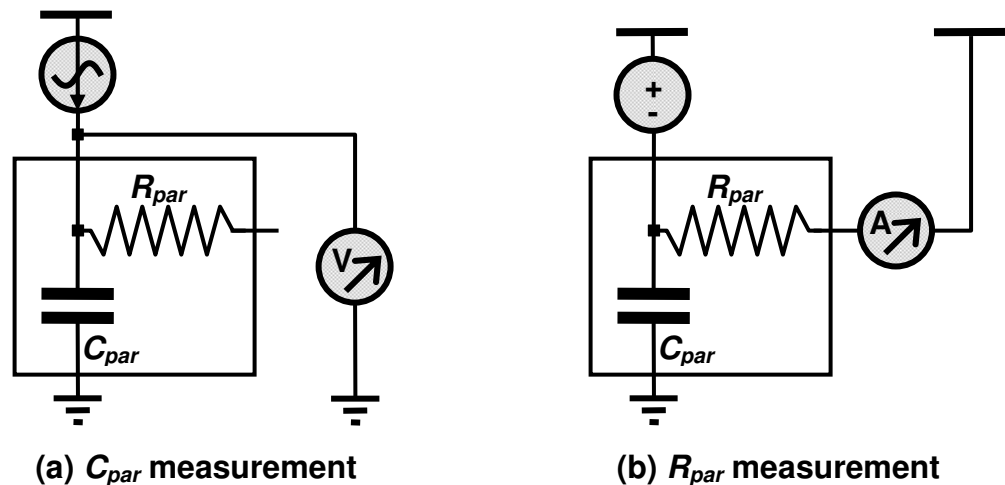
The dynamic current waveforms are acquired by performing a transient analysis as shown in figure 4.1. This setup is identical to that used for

timing characterization; therefore you can perform timing and power characterization simultaneously.

5.3 Equivalent Parasitics

You can obtain the equivalent capacitance by performing a simple AC analysis in the DC operating points obtained during SD leakage analysis. By applying an AC voltage source to the PG pin and measuring the resulting AC current, you can derive the capacitance (shown in figure 5.1a).

Figure 5.1: Characterization of Equivalent Parasitics



An easy way to measure the equivalent resistance is to perform a second DC analysis with a slightly different voltage on the PG pin and with the output tied to a voltage source with the original DC output voltage, as shown in figure 5.1b. Calculate the equivalent resistance from the current supplied by the voltage source at the output.

6 Advanced Modeling & Support

This section describes gate leakage modeling, asynchronous operation modeling and voltage/temperature scaling.

6.1 Gate Leakage Modeling

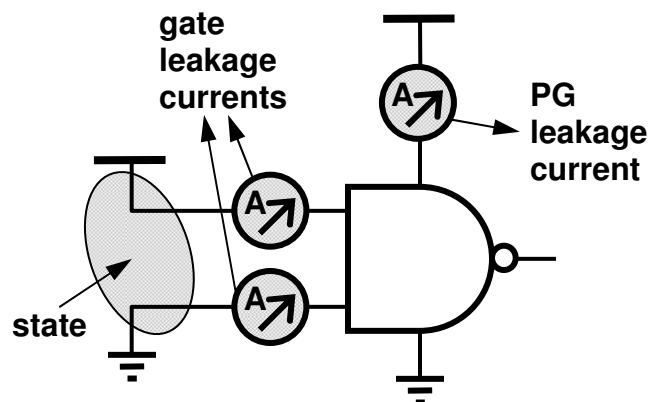
While gate leakage current is quite insignificant in 100nm and higher technologies, it will gradually become a more significant current component in more advanced technology nodes. If a library developer chooses to include gate leakage current data in the library, the characterization process should be adjusted accordingly.

Gate leakage is defined as a static current from a driver cell to transistor gates in a load cell. If the gate is driven high, the current flows from the power pin of the driver cell by way of the gate to the ground pin of the load cell. The current can also flow back from the power pin on the load cell via the gate to the ground pin of the driver cell.

During the characterization process the leakage currents on the input and power/ground pins are measured for the cell in an open configuration, that is, with outputs that do not drive other cells. It is important that the cells's outputs do not conduct static current during the measurement.

The leakage currents are state dependent. The leakage current measurement is very similar to the measurement for the conventional model with only channel leakage: for combinational cells the inputs are driven at certain levels depending on the state, while for sequential cells a sequence of states may be required to bring the cell to a certain state. Once the transition is complete, the currents on the power/ground pins and input pins are measured.

Figure 6.1: Gate Leakage Measurement



The direction of the current depends on the state of the input pin that is connected to the transistor gates. The magnitude of the current depends on the state of the other input pins of the load cell. During leakage power measurement you can measure the gate leakage currents on the input pins together with the channel leakage currents on the PG pins, as shown in figure 6.1. It is important to note that this measurement should be performed with open output pins so that no current is drawn from the outputs.

Current conservation still holds, but now the gate leakage of the input pins must be taken into account as well:

$$\sum_{pg_pin} I_{leak}(pg_pin) + \sum_{pg_pin} I_{leak}(input_pin) = 0 \quad (6.1)$$

When a cell is present in a netlist, the output currents will not be zero. Instead, a certain constant current will be supplied to maintain the gate leakage of the driven cell. The application adds the gate leakage current of the driven cell to the power/ground pins of the driving cell to calculate the actual leakage currents in operation.

6.2 Asynchronous Operation Modeling

For memory modeling, basing the models on single-input events works well for synchronous events because they are triggered by a toggle on a single `read_enable` or `write_enable` that acts as a clock signal. However, for asynchronous read access the event is triggered by a change on the address bus. More than one bit of the address bus could be toggling, but the result is still considered a single (read) event.

For certain cells the typical operation is characterized by simultaneous switching input events. For these cells the power dissipation is mostly independent of how many inputs changed, as long as at least one of the inputs changed. For example, for an asynchronous RAM cell any new address will cause a new column to be selected in the RAM, which will trigger a new read operation.

This type of power dissipation cannot be modeled as a single-input event because the magnitude of the component is independent of the number of inputs that toggled. as long as they toggled within a certain time frame (the access time of the RAM). The power consumption is triggered by a state change on a multibit pin group within a certain time frame.

CCS Power can model asynchronous RAM cells and other types of complex cells that exhibit asynchronous operation by adding an attribute to specify the number of bits in the input bus that are switching.

6.3 Voltage and Temperature Scaling Support

CCS Power enables scaling for intermediate Vdd and temperature values. Library characterization occurs for a small number of Vdd values with advanced current waveform interpolation at runtime. Use the calculations for any instance-specific value in a continuous range of Vdd, which is a key element for flows that consider the effect of IR drop. This also supports multi-Vdd and DVFS (Dynamic Voltage and Frequency Scaling) designs. In addition, CCS Power scaling supports power calculation for arbitrary temperature values between characterization points.

7 Conclusion

CCS Power unifies the library data for power and rail analysis and optimization, ensuring consistent analysis and simplification of the analysis flow. By capturing current waveforms in the library, you can extend the entire tool suite to increase the time resolution of analysis and provide more accurate identification of potential problem areas. By providing a comprehensive solution for dynamic and leakage power, multivoltage design and sign-off power analysis, CCS Power meets the power challenges for today's designs.

CCS Power is the underlying method for the next generation of power synthesis and analysis tools and is critical to the success of 90nm designs, 65nm designs, and beyond.